

3. Processor Research Team

3.1. Team members

Makoto Taiji (Team Leader)
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3.2. Research Activities

The aim of the processor research team is to create a future basis of high-performance processors for scientific simulations, as well as to explore the processor performance of the K computer.

In future high performance computing, we have to tackle with millions or more parallel operation units to extend the performance. However, many applications require acceleration while keeping the problem size, i. e. the strong scaling, and they can often be parallelized up to thousands of core, not to millions. To achieve better strong scaling, we have to decrease the cost of parallelization by improving the latency in everywhere – network, main memory, and processors. For this, we will try to develop the platform of System-on-Chip (SoC) based accelerators. It consists of general-purpose processor cores, memories, network units and computing accelerators on the single chip. By such integration we aim to achieve the ultimate performance for selected applications.

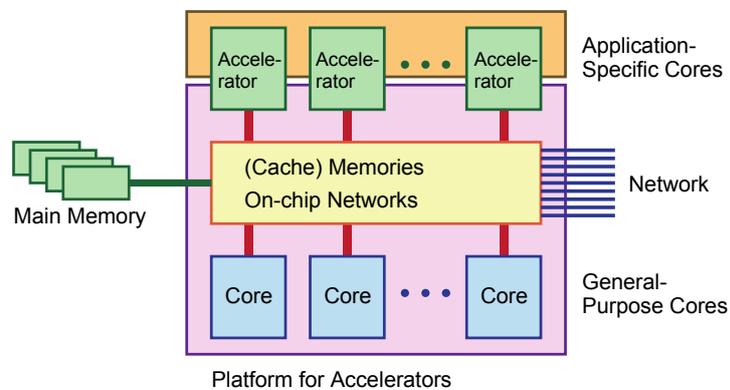


Figure 1. Diagram of platform for accelerators.

In addition to the researches on future computing platform, we will contribute to accelerate the application performance on the K computer. The processor of K computer, SPARC64 VIIIfx, has several special features for high-performance computing called VISIMPACT and HPC-ACE. We will explore to extract its power for several applications based on our experience on the processor architecture.

3.3. Research Results and Achievements

3.3.1. Platform of accelerators

In this year we have designed the MDGRAPE-4 SoC in RIKEN QBiC (Quantitative Biology Center). From the viewpoint of the platform of SoC based accelerator, we can use as the MDGRAPE-4 SoC as the basis. It has 64 processor units, 64 dedicated pipelines for molecular dynamics force calculation, main memories, and network units for 3-dimensional torus network. By replacing the dedicated pipelines we can use the design as the platform of accelerators.

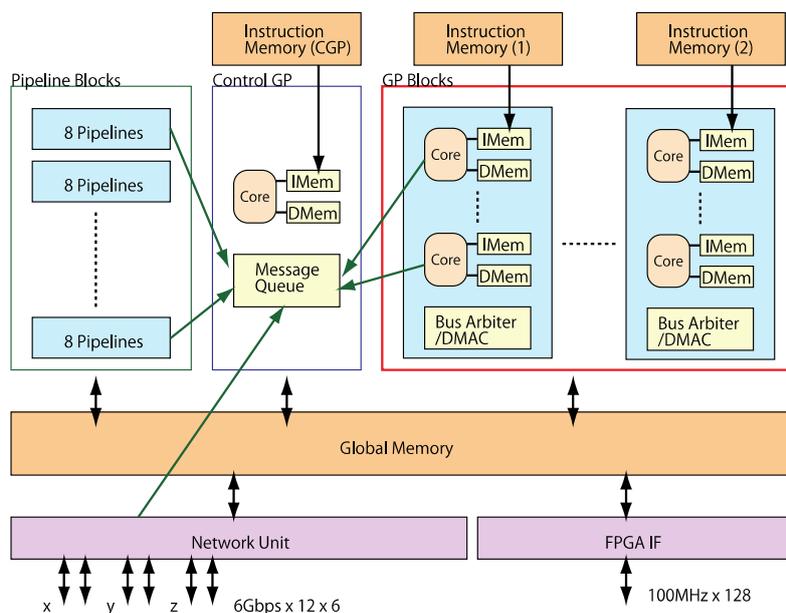


Figure 2. Block diagram of MDGRAPE-4 SoC.

3.3.2. Application Optimization on K computer

For application optimization we have started the optimization of the molecular dynamics core code.

3.4. Schedule and Future Plan

In the next year, we will finish the design of the MDGRAPE-4 SoC in RIKEN QBiC. In the team we will implement the part of the MDGRAPE-4 SoC as the platform of accelerators. We will also develop simulation environments for such system at RTL-level and behavior level. We will continue the optimization of MD core and the other codes for the K computer.