分野 2 CMSI

実空間密度汎関数法による ナノ物質の第一原理 シミュレーション

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科

実空間密度汎関数法コード - RSDFT-

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筑波大(櫻井研)二村保徳(櫻井-杉浦の固有値解法)

- 東大(押山研) 内田和之(二層グラフェン)
- 東大(押山研) 澤田啓介(SiCステップ表面)

Computer Science Material Science



ACM Gordon Bell Prize Peak Performance

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First-Principles Calculation of Electronic States of a Silicon Nanowire with 100,000 Atoms on the K Computer





Hand D. December Jr. Thom II. Dunning, Jr. Gordon Bell Chair





- 第一原理電子状態計算
 - 密度汎関数法
 - RSDFT
- Siナノワイヤ
- 櫻井-杉浦法のバンド構造計算への応用(筑波大 二村保徳)
- 捩じれた二層グラフェン(東大内田和之)
- SiCステップ表面(東大 澤田啓介)
- RSDFT-CPMDの実装(東大小泉健一)

FIRST-PRINCIPLES CALCULATIONS

Density Functional Theory

LARGE-SCALE FIRST-PRINCIPLES CALCULATIONS IN NANO WORLD



Large-scale DFT calculations and experiments meet together in Nano World !

Challenge: 10,000 ~ 100,000-atom calculations overcoming N³ scaling to reveal nano-scale world!

DENSITY FUNCTIONAL THEORY

Energy functional

$$E[\{\phi_i\}] = \sum_{i=1}^{N} \int d\mathbf{r} \phi_i^*(\mathbf{r}) \left(-\frac{1}{2} \nabla^2 \phi_i(\mathbf{r}) \right) \quad \text{index} + \mathbf{r}$$

+
$$\int d\mathbf{r}
ho(\mathbf{r}) v_{ion}(\mathbf{r})$$
電子-イオン相互作用

+
$$\frac{1}{2}\int d\mathbf{r}\int d\mathbf{r}' \frac{\rho(\mathbf{r})\rho(\mathbf{r}')}{|\mathbf{r}-\mathbf{r}'|}$$
電子間クーロン相互作用

+ $E_{xc}[
ho]$ その他量子力学的効果 (交換相関効果) Electron density $ho(\mathbf{r}) = \sum_{i=1}^{N} \left|\phi_i(\mathbf{r})\right|^2$ electron ion

P. Hohenberg and W. Kohn, Phys. Rev. 136 (1964) B864.

W. Kohn and L. J. Sham, Phys. Rev. 140 (1965) A1133.

KOHN-SHAM EQUATION







M. T. Yin and M. L. Cohen, Phys. Rev. B26, 5668 (1982).



DFT CALCULATION IN REAL-SPACE GRID METHOD

RSDFT

REAL-SPACE FINITE-DIFFERENCE PSEUDOPOTENTIAL METHOD FFT free



$$\left(-\frac{1}{2}\nabla^2 + \hat{v}_{ion} + \int d\mathbf{r}' \frac{\rho(\mathbf{r}')}{|\mathbf{r} - \mathbf{r}'|} + \frac{\delta E_{xc}[\rho]}{\delta \rho(\mathbf{r})}\right) \phi_j(\mathbf{r}) = \varepsilon_j \phi_j(\mathbf{r})$$

Kohn-Sham equation is solved in discretized space

J. R. Chelikowsky *et al.*, Phys. Rev. B50, 11355 (1994). J.-I. Iwata *et al.*, J. Comp. Phys. 229, 2339 (2010).

> Derivatives \rightarrow (higher-order) finite difference

$$\frac{\partial^2}{\partial x^2}\phi(\mathbf{r}) \approx \sum_{m=-6}^{6} C_m \phi(x + m\Delta, y, z)$$

$$\blacktriangleright \text{ Integrals} \rightarrow \text{summation over grid points } \int \phi_m^*(\mathbf{r})\phi_n(\mathbf{r})d\mathbf{r} \approx \sum_{i=1}^{N_{grid}} \phi_m^*(\mathbf{r}_i)\phi_n(\mathbf{r}_i)\Delta V$$

► Ionic potentials → Pseudopotentials $\hat{v}_{ion} = v_{local}(\mathbf{r}) + \sum_{a,l,m} |\beta_{alm}\rangle\langle\beta_{alm}|_{N.}$

N. Troullier & J. L. Martins Phys. Rev. B 34, 1993 (1991)

GRID, BAND, k, SPIN PARALLELIZATION

 ◆ MPI (Message-Passing Interface) library MPI_ISEND, MPI_IRECV → finite-difference calc. MPI_ALLREDUCE → global summation

OpenMP

Further grid parallelization (within each CPU) is performed by thread parallelization



Example of CPU allocation for 4-grid, 2-orbital, 2-k, 1-spin parallelization



計算上の問題点

SiNW110 (20nm 6309 atoms 3600 nodes	diameter)	ML=660 x MB=1344 4 sample	660 x 12 0 k points		(s	second)
	SCF		DIAG	GS	CG	
Env_base_1.2.0-07						
Env_base_1.2.0-09						
Env_base_1.2.0-09 (with mca options)						

Details of DIAG routine

(second)

	DIAG	mate	hpsi	pdsyevd	rotv
Env_base_1.2.0-07					
Env_base_1.2.0-09					
Env_base_1.2.0-09 (with mca options)				We found MPL BC	AST is the downfal

NATORI'S COMPACT MODEL FOR BALLISTIC SI NANOWIRE MOSFET

NEW TRANSISTOR STRUCTURES - SUPPRESSION OF OFF-LEAK CURRENT -



Power consumption by off-leak current substantially increases as scaling down of planer FET



Gate controllability \rightarrow suppress leaks at off state

 \rightarrow reduce power consumption

Surrounding-gate transistor

Silicon Nanowire is the most promising channel material for SGFET

シリコンナノワイヤの原子構造 (100)断面



CROSS SECTIONAL VIEWS OF SINWs



D=1.96nm	D=1.94nm	D=1.93nm
[001]	[011]	[111]

BAND STRUCTURE OF SINW

 $\left(-\frac{1}{2}\nabla^2 + v_{SCF}(\mathbf{r}) + i\mathbf{k}\cdot\nabla + \frac{k^2}{2}\right)\psi_{n\mathbf{k}}(\mathbf{r}) = \varepsilon_{n\mathbf{k}}\psi_{n\mathbf{k}}(\mathbf{r})$



n番目の状態にある電子の速度

$$\frac{d\varepsilon_n(k)}{dk} = \left\langle \psi_{nk} \right| - i\nabla \left| \psi_{nk} \right\rangle$$

Derivative of the band energy was calculated by r.h.s. of the following formula

コンパクトモデルによる 電流-電圧特性の評価



NUMBER OF CARRIERS IN THE CHANNEL



NUMBER OF CARRIERS IN THE CHANNEL



$$Q_e^{Channel} = q \left(N_e^{Fore} + N_e^{Back} \right)$$

$$C_g = \frac{\mathcal{E}_{OX}}{2\ln\left(\frac{R+t_{OX}}{R}\right)}$$

$$Q_e^{Channel} = C_g \phi_g$$

$$\phi_g = V_g - V_{th} - \frac{\mu_s - E_{CBM}}{q}$$

CURRENT FORMULA

$$I_{d} = 2q \sum_{n} \int_{\frac{dE_{n}(k)}{dk} > 0} \frac{dk}{2\pi} \frac{1}{h} \frac{dE_{n}(k)}{dk} \frac{1}{1 + \exp\left(\frac{E_{n}(k) - \mu_{s}}{kT}\right)}$$
$$+ 2q \sum_{n} \int_{\frac{dE_{n}(k)}{dk} < 0} \frac{dk}{2\pi} \frac{1}{h} \frac{dE_{n}(k)}{dk} \frac{1}{1 + \exp\left(\frac{E_{n}(k) - \mu_{d}}{kT}\right)}$$

$$= \frac{q}{\pi h} \sum_{n} \int dE_{n} \frac{1}{1 + \exp\left(\frac{E_{n} - \mu_{s}}{kT}\right)} - \frac{q}{\pi h} \sum_{n} \int dE_{n} \frac{1}{1 + \exp\left(\frac{E_{n} - \mu_{d}}{kT}\right)}$$
$$= \frac{q}{\pi h} \sum_{n} \int dE_{n} \left(f(E_{n}, \mu_{s}) - f(E_{n}, \mu_{d})\right)$$

Landauer formula

$$I = \frac{q}{\pi h} \sum_{n} T_n(E) \int dE \left(f(E, \mu_s) - f(E, \mu_d) \right)$$

CALCULATION PROCEDURE

Perform band calculation

$$\left(-\frac{\mathsf{h}^2}{2m}\nabla^2 + v(\mathbf{r})\right)\psi_{nk}(\mathbf{r}) = E_n(k)\psi_{nk}(\mathbf{r})$$

Get

$$\begin{bmatrix}
E_n(k) \\
\frac{1}{h} \frac{dE_n(k)}{dk} = \frac{1}{m} \langle \psi_{nk} | -ih\nabla | \psi_{nk} \rangle$$

Give V_g - V_{th} and V_{ds} as input parameters, and solve the following equation

$$\begin{bmatrix} C_g \left(V_g - V_{th} - \frac{\mu_s - E_{CBM}}{q} \right) = Q_e^{Channel} = q \left(N_e^{Fore} + N_e^{Back} \right) \\ N_e^{Fore} = \sum_n 2 \int_{\frac{dE_n(k)}{dk} > 0} \frac{dk}{2\pi} \frac{1}{1 + \exp\left(\frac{E_n(k) - \mu_s}{kT}\right)} \\ N_e^{Back} = \sum_n 2 \int_{\frac{dE_n(k)}{dk} < 0} \frac{dk}{2\pi} \frac{1}{1 + \exp\left(\frac{E_n(k) - \mu_d}{kT}\right)} \\ \mu_d = \mu_s - qV_{ds} \end{bmatrix}$$

CALCULATION PROCEDURE

Calculate the drain current by the following formula

$$I_{d} = 2q \sum_{n} \int_{\frac{dE_{n}(k)}{dk} > 0} \frac{dk}{2\pi} \frac{1}{h} \frac{dE_{n}(k)}{dk} \frac{1}{1 + \exp\left(\frac{E_{n}(k) - \mu_{s}}{kT}\right)}$$
$$+ 2q \sum_{n} \int_{\frac{dE_{n}(k)}{dk} < 0} \frac{dk}{2\pi} \frac{1}{h} \frac{dE_{n}(k)}{dk} \frac{1}{1 + \exp\left(\frac{E_{n}(k) - \mu_{d}}{kT}\right)}$$



SiNW(100) diameter : 2nm temperature : 300K SiNW(110) diameter : 2nm temperature : 300K SiNW(111) diameter : 2nm temperature : 300K







SiNW(100) diameter : 4nm temperature : 300K SiNW(110) diameter : 4nm temperature : 300K SiNW(111) diameter : 4nm temperature : 300K



CONTOUR PLOT OF CURRENT DENSITY By S. Furuya (VESTA)

 $V_{g} = 0.1 V$ $V_{g} = 0.7 V$



BAND STRUCTURE CALCULATIONS WITH SAKURAI-SUGIURA METHOD

二村保徳 ^{筑波大} 櫻井研

SCF CALCULATIONS AND BAND CALCULAITONS



SAKURAI-SUGIURA METHOD

- A novel eigensolver
 - Suitable for interior eigenproblems
 - Suitable for massively-parallel architectures

Band structure calculation of 10,000-atom system

CONTOUR INTEGRATION

$$S_{k} \equiv \frac{1}{2\pi \mathrm{i}} \int_{\Gamma} z^{k} (zI - A)^{-1} \bigvee_{\uparrow} \mathrm{d}z$$

$$\downarrow \text{ arbitrary vectors} \text{ (linearly independent)}$$

$$S_{k}, \bigvee C^{n \times L}$$

$$k = 0, 1, \dots, M - 1$$

$$L, M << n$$

$$\downarrow \text{ of grid points}$$

BAND STRUCTURE OF 10,000-ATOM SiNW



ATOMIC & ELECTRONIC STRUCTURES OF TWISTED BILAYER GRAPHENE

内田和之 _{東大押山研}



*Assumption: In the above and following, an A-site atom is on the twist axis in each graphene. Other cases will be also discussed later (consideration of lateral translations).

Why tBLG?





Atomic-structure Optimization



Relation between Corrugations and Stacking Structures







 $\theta < \sim 20^{\circ}$

Corrugation

Locally AA/AB stacked regions exist, and become larger as θ becomes smaller

澤田啓介 _{東大押山研}

FIRST-PRINCIPLES CALCULATIONS OF STEP STRUCTURES ON SiC(0001)

Silicon-Carbide



 Silicon#arbide#(SiC)#s#hopeful#semiconductor#for# the#next#genera4on#of#power-electronic-device.



Features#and#applica4ons#of#SiC#semiconductors.

Template-of-Nanostructures-using-Step-Structures

• Step structures can be applicable to the template-ofnanostructures such as nano wires, tubes and dots.



J. Y. Son et al., Electrochem. Solid-State Lett. **14**, H397 (2011).



Nanofacet on 4H-SiC(0001) is applied to template of the field-effect transistor using self-organized graphene nanoribbon. The fabrication of ZnO nanowires is demonstrated on steps of sapphire $[Al_2O_3 (0001)]$ surface.

• SiC基板の熱分解によるグラフェン生成

Morphologies-of-Vicinal-Solid-Surface

- It is important to understand structures of surfaces or interfaces on substrates for the device fabrications.
- Vicinal solid surface often shows regularly spaced step,-terrace-and-nanofacet-formed by step bunching.

A. Nakajima et al., J. Crystal Growth **278**, 437 (2005). AFM image of 6H-SiC substrate surface.



E. D. Williams et al., Surf. Sci. **294**, 219 (1993). STM image of Si(111) surface.





Expected-Simple-Step-Structures

Cross&ec1onal-TEM-image



Single-height&tep-(SHS)-structure-



Double-height&tep-(DHS)-structure-

Quad-height&tep-(QHS)-structure





- コンパクトモデルを用いたSiNW-FETの電流電圧特性の計算
 - ゲート電極の効果を第一原理的に扱う(産総研大谷実)
 - ソース・ドレイン電極も取り入れた第一原理輸送計算 (東大押山研 Zixin Guo、東大渡邊研 笹岡健二)
 - 第一原理デバイスシミュレータ
- 捻れ二層グラフェンの構造と電子状態(東大押山研内田和之)
- SiC微斜面の構造決定(東大押山研 澤田啓介)

■ 機能拡張

RSDFT-CPMDの実装(東大押山研小泉健一、阪大重田照育)